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(71) Applicant: **Paradyne Corporation**
Largo, Florida 33773 (US)

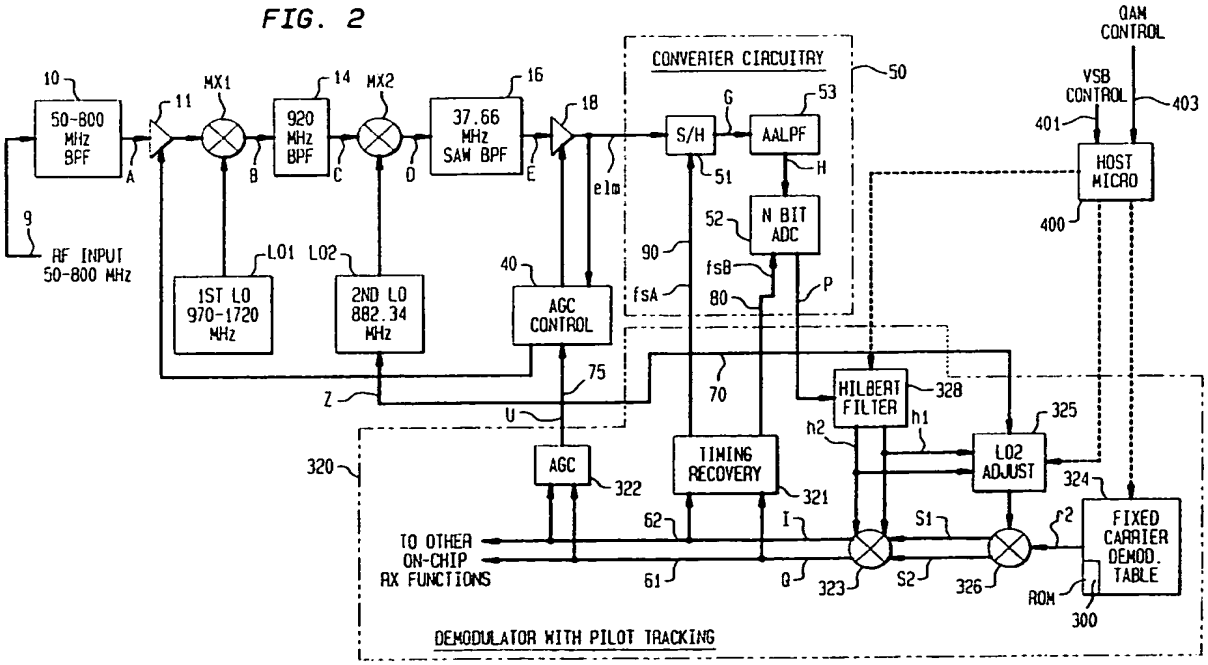
(72) Inventor: **Cupo, Robert L.**
Eatontown, New Jersey 07724 (US)

(74) Representative: **Jehan, Robert et al**
Williams, Powell & Associates,
34 Tavistock Street
London WC2E 7PB (GB)

(54) Radio frequency receiver adapted to receive one or more modulated signals

(57) A radio frequency (rf) receiver adapted to receive a number of different digitally modulated rf input signals such as quadrature amplitude modulated (QAM) and vestigial side band (VSB) rf input signals includes circuitry (11-18) for down converting the rf input signals to an intermediate frequency (IF) range having a centre frequency fc2 and a bandwidth of Bhz and converter circuitry (50) for sampling the IF signals and then producing corresponding baseband signals. In a preferred embodiment, the intermediate frequency signals are applied to a sample and hold circuit (51) which is sampled at a frequency fs and whose output is coupled via a low pass filter (53) to an analog-to-digital converter (52) whose output is then applied to a Hilbert filter (328) for demodulating the sampled signals and producing baseband signals. In-phase (I) and quadrature (Q) signals are produced whose phase and amplitude are not a function of different components and their tolerance of different conduction paths.

FIG. 2



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Description

This invention relates to a radio frequency (rf) receiver.

To better understand the field of the invention reference is made to FIG. 1 which shows a portion of a prior art conventional TV receiver with baseband sampling for vestigial side band (VSB) or quadrature amplitude modulation (QAM) mode of operation. This receiver employs a synchronous detector and an analog pilot tone recovery loop shown in block 20 of FIG. 1. For a VSB signal, only one channel (i.e., the I channel, including mixer 21, filter 28 and ADC 29) is needed, requiring only one analog-to-digital (i.e., ADC 29) converter. However, a substantial amount of circuitry is required for implementing the synchronous detector, as is evident from an examination of block 20 shown in FIG. 1.

In FIG. 1, received rf input signals 9 are propagated via a first band pass filter (BPF 10), an amplifier (AMP 11), a first mixer (MX1) which mixes the output of AMP 11 with the output of a first local oscillator (LO1), a second band pass filter (BPF 14), a second mixer (MX2) which mixes the output of BPF 14 with the output of a second local oscillator (LO2), a third band pass filter (BPF 17) and an IF amplifier 18 to produce an IF signal, el, present at the output of amplifier 18. In FIG. 1, the IF output will have a bandwidth of 6 MHz, centred around 44 MHz. The IF signal el is supplied to one input of a mixer 21 having another input to which is applied an output of a third local oscillator (LO3). The output of mixer 21 which is defined as the in-phase (I) signal is applied to the input of an anti-aliasing low pass filter (AALPF) 28. The output of AALPF 28 is then applied to an N-bit analog-to-digital converter (ADC) 29. The output of ADC 29 is applied to an input port of a baseband demodulator chip 32. In addition, a pilot low pass filter (Pilot LPF) 24, has an input connected to the I output of mixer 21, and an output connected to an input of a limiter 25 having an output connected to an input of a mixer 26.

When quadrature amplitude modulation (QAM) mode is present and needs to be decoded, another problem arises. Since QAM has an in-phase (I) input and a quadrature (Q) baseband input, a second analog channel and a second AID converter are required to decode the input data. This is shown in FIG. 1, where the signal el is applied to one input of a mixer 22 having another input connected to an output of the LO3 for producing the quadrature (Q) output signal. The Q signal is applied to an input of an anti-aliasing low pass filter (AALPF) 31 whose output is applied to an input port of an N-bit analog-to-digital converter, 30. ADC 29 and 30 function to sample the signal in the baseband frequency range. The baseband I_B output of ADC 29 and the baseband Q_B output of ADC 30 are then applied to the inputs of a timing recovery circuit 34 and to the inputs of an AGC circuit 35 located within demodulator 32.

The analog pilot loop includes mixing the Q output from mixer 22 and the I output derived from limiter 25 in a mixer 26 whose output is applied to the input of a pilot low pass filter (LPF 27). The output of pilot LPF 27 is an analog signal which is applied to, and controls, the second local oscillator circuit, (LO2). Analysis of the prior art circuit indicates the existence of several problems.

First, there is a problem related to the complexity of the synchronous detector components required to produce the I and Q functions.

Secondly, there exists a distinct possibility that the two analog channels (mixer 21 and AALPF 28; mixer 22 and AALPF 31) will have different responses to the amplitude and phase of the signals being propagated due to component tolerances of the mixers and filters. This will have a negative impact on the quality of performance. A solution to this problem was suggested in an article entitled Asymmetric Baseband Equalization by Hikmet Sari and Georges Karam (IEEE Transactions on Communications, Vol. 36, No. 9, September, 1988). However, this reference suggests the use of an asymmetric structure which requires twice as many taps as a conventional symmetric equalizer as well as twice the adaptation control.

Note that the prior art, as shown in FIG. 1, teaches the sampling of the baseband stage (i.e., the outputs of AALPF 28 and 31). Sampling at the baseband level suffers because of:

a-quadrature imperfections on the modulator carriers;
b-amplitude imbalance between the I and Q baseband analog channels; and
c-phase imbalance between the I and Q baseband analog channels.

The present invention seeks to provide an improved radio frequency receiver.

According to an aspect of the present invention, there is provided a radio frequency receiver as specified in claim 1.

According to another aspect of the present invention, there is provided a radio frequency receiver as specified in claim 15.

The preferred embodiments can provide improved reception with a system which is simpler in that it uses fewer components, and which avoids the problem of producing and propagating the I and Q signals along two different paths which introduce different phase and amplitude factors into the signal.

Preferred systems include means for controlling the tuner and IF stages of the front end of a high definition television (HDTV) receiver to enable the receiver to handle both vestigial side band (VSB) and quadrature amplitude modulated (QAM) schemes of digital modulation.

Advantageously, the output of an IF stage is sampled as compared to the sampling of the baseband stage, as is typically done in the prior art.

The preferred embodiments can eliminate the need

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for much of the synchronous detector circuitry found in the prior art. This can eliminate the cost of rather expensive circuitry. Also and perhaps more important is that both the VSB and QAM signals preferably pass through and along the same analog channel. This eliminates the presence of two different paths which introduce different delays and different gain factors to incoming signals.

In a preferred embodiment, in the converter, the clocking frequency applied to the sample and hold circuit is two times the clocking frequency applied to the analogue to digital converter.

A preferred embodiment provides a radio frequency (rf) receiver adapted to receive one, or more, of a number of differently modulated rf input signals including quadrature amplitude modulated (QAM) and vestigial side band (VSB) rf input signals comprising a first mixer having an input means to which is coupled the rf input signals and an output of a first local oscillator and wherein the first mixer has an output which is applied to an input of a first bandpass filter (BPF1) having a first centre frequency (fcl) and a bandwidth of Bhz to produce at an output of BPF1 a first output signal (fol) having a first centre frequency of fcl with a bandwidth of Bhz; a second mixer for down converting the rf signal having an input means to which is coupled the output of BPF1 and an output of a second local oscillator; the second mixer having an output coupled to an input of a second bandpass filter (BPF2) having a second centre frequency (fc2) and a bandwidth of Bhz; the BPF2 having an output for producing thereat an intermediate frequency signal whose centre frequency is equal to fc2 and whose bandwidth is equal to Bhz; converter means including sampling means and demodulating means for digitally sampling the intermediate frequency signal at a sampling rate (fs) and for producing a baseband signal, corresponding to the particular rf input signal received, having a centre frequency fc3; and wherein fc3 and fc2 are rational multiples of each other.

Preferably, in this embodiment, the demodulating means includes a look-up table including values of demodulating angles for producing in-phase (I) and quadrature (Q) baseband signals in response to a QAM rf input signal and for producing in-phase baseband signals in response to a VSB rf input signal.

An embodiment of the present invention is described below, by way of example only, with reference to the accompanying drawings, in which:

FIGURE 1 is a block diagram of a high definition TV (HDTV) receiver with baseband sampling in accordance with the prior art;

FIGURE 2 is a block diagram of a portion of an embodiment of HDTV receiver with sampling of the IF stage;

FIGURE 3 is a diagram of waveshapes associated with the circuit of FIGURE 2; and

FIGURE 4 is a block diagram of a portion of another embodiment of HDTV receiver with sampling of the IF stage.

FIGURE 2 shows in block form a system embodying the invention. The input section of the receiver is similar to the prior art input section. That is, the RF input 9 comprising signals ranging from 50 to 800 MHZ is applied to a band pass filter 10 whose output "A" is applied to the input of an amplifier stage 11 whose gain is controlled by means of an automatic gain control (AGC) circuit 40. The output of Amplifier 11 and the output of a first local oscillator, LO1, are applied to a first mixer, MX1. The output "B" of mixer MX1 is applied to the input of a 920 MHz bandpass filter 14. The section just described is identical to the prior art circuitry shown in FIG. 1.

In Fig.2, the output "C" of bandpass filter 14 and the output of a second local oscillator, LO2, are supplied to a second mixer, MX2, where they are mixed. The output "D" of mixer MX2 is supplied to the input of a bandpass filter 16. In Fig. 2, the centre frequency of LO2 is 882.34 MHz and bandpass filter 16 is designed to have a centre frequency of 37.66 MHz. The significance of the selection of the centre frequency of 882.34 MHz for LO2 and the selection of the centre frequency of bandpass filter 16 to be 37.66 MHz is discussed below. The output, E, of bandpass filter 16 is applied to an input of an IF amplifier 18, whose gain is controlled by one or more signals from AGC circuit 40. The output, elm, of amplifier 18 is applied to the input of a converter circuit 50. The signals E and elm lie within a frequency band centred about 37.66 MHz, as shown for the waveform in FIG. 3 identified as IF OUT.

Referring back to FIG. 2, elm is applied to the input of a sample and hold (S/H) circuit 51, operated at a sampling rate of 43.04 million samples per second (MSPS). Sample and hold circuit 51 may be, for example, a circuit such as the Analog Device AD 9101, or any similarly available or like circuit. The output G of S/H 51 has a spectrum as shown in Fig. 3 identified as S/H OUT. As shown in Fig. 3, the IF OUT band of signals centred at 37.66 MHz is translated down to a centre frequency of 5.38 MHz with a mirror image with a centre frequency of -5.38 MHz. The bandwidth of the signal extends ±2.69 MHz about the centre frequency. Note that the S/H output also includes a band of signals having a centre frequency of 37.66 MHz with a mirror image having a centre frequency at 48.42 MHz. The S/H output also includes a band of signals having a centre frequency of -37.66 MHz and -48.42 MHz, respectively. Note also that, as shown in Fig. 3, there may be a pilot tone (PT) signal shown by a vertical arrow.

The output (G) of S/H 51 is applied to the input of an antialiasing low pass filter (AALPF) 53 to produce an output (H) which has a spectrum identified as AALPF OUT in Fig. 3. The filter 53 eliminates all signals outside of the signals having a centre frequency of 5.38 MHz and the mirror image having a centre frequency of -5.38

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MHz. The output (H) of filter 53 is applied to the input of an N-bit analog to digital converter (ADC) circuit 52 which is operated at a conversion or sampling rate of 21.52 MSPS. ADC 52 may be, for example, a 10-bit ADC such as the SPT 7855 made by Signal Processing Technologies or any similarly available or like designed circuit. The output (P) of A/D converter 52 has the frequency response shown in the waveform identified as A/D OUT in Fig. 3. Since the periodic repetitions in A/D OUT do not overlap, the sampling process of the A/D converter has no aliasing.

S/H 51 is operated at a 43.04 MHz rate even though the signal bandwidth is only 6 MHz because S/H 51 must be rated for signals that have a frequency content lying in a range between 34-40 MHz. Thus, one cannot simply use an A/D converter which samples at twice the bandwidth of the 6MHz signal band (12 MHz) when such a high centre frequency (i.e., 37.66 MHz) exists.

Thus while S/H 51 is sampled at a 43.04 MHz sampling rate, as stated above, a 43.04 MHz analog-to-digital conversion rate is not required. S/H 51 functions to translate the IF centre frequency from 37.66 MHz to 5.38 MHz via the sampling process. As shown in the S/H OUT waveform of Fig. 3, the bandwidth of the translated S/H output signal (G) will extend up to 8.07 MHz and down to 2.69 MHz. Thus, an A/D sampling rate of 21.52 MHz (controlled by signals from circuit 321 supplied on lead 80) will satisfy the Nyquist criteria.

In the circuit of Fig. 2, two sampling rates are used; one sampling rate (43.04 MHz) is used for S/H 51 and another sampling rate (21.52 MHz) is used for A/D converter 52. Therefore, an antialiasing low pass filter (AALPF) 53, is inserted between the output of S/H 51 and the input to ADC 52. This ensures that the A/D converter sampling process sees no energy beyond 10.76 MHz, to satisfy the Nyquist criteria of ADC 52. Thus, in Fig. 2, a 43.04 MHz sampling clock is supplied to S/H 51 via line 90 and a 21.52 MHz sampling clock is supplied to ADC 52 via line 80. In contrast, in the baseband scheme of Figure 1, two (2) ADC converters (29 and 30) are required, with a sampling clock which could be as low as 10.76 MHz being supplied to both ADC 29 and 30 via line 85.

A comparison of Figures 1 and 2 reveals that the synchronous detector 20 of Fig. 1 has been effectively replaced by a sample and hold circuit 51 and that the system of Figure 2 requires only one N bit A/D converter for either VSB or QAM.

The problems associated with the prior art system of FIG. 1 have been eliminated and there is, also, no need for an asymmetric equalizer.

Therefore, in systems embodying the invention, the complexity of the circuitry can be reduced and the performance can be improved, at the same time. However, it should be noted that the system of FIG. 2, requires that the demodulator 320 be different than the demodulator 32 used in FIG. 1. The differences may be noted by comparing the front end of the demodulator of Figure 1 with that shown in Figure 2. The demodulator 320 of Fig. 2 includes a Hilbert filter 328, a timing recovery circuit 321, an AGC circuit 322, a demodulator 323, an LO2 adjustment circuit 325, a summer 326 and a fixed carrier demodulation table 324. The Hilbert filter is needed to accurately produce the quadrature related signals I and Q produced for the QAM mode.

The N-bit output, P, from ADC 52 is applied to an input of Hilbert filter 328. Hilbert filters are known in the art and are discussed, for example, in "Digital Signal Processing", A. Oppenheim and R. Schafer, Ch. 7, Prentice Hall, 1975; and "Theory and Application of Digital Signal Processing", L. Rabiner and B. Gold, pp. 71-72, Prentice Hall, 1975.

The Hilbert filter 328 may be generated by standard design procedures. The output (P) of ADC 52 is applied to the input of Hilbert filter 326 which has two outputs (hI, h2), with the hI output representing the real component of the filter output and the h2 output representing the quadrature component of the filter output with h2 output being used for QAM. For the VSB mode, h2 can be set to zero thereby removing any imaginary channel. The hI and h2 outputs of the Hilbert filter may be used to adjust the frequency of the second local oscillator LO2. As shown in FIG. 2, h1 and h2 are applied to the input of an L02 adjustment circuit 325 having an output 2 which is supplied via line 70 to LO2. The application of the output Z signal functions to remove frequency offset within the selected channel in predetermined quantization steps of, for example, 60KHz.

The Hilbert filters function generally as follows: One output (e.g., hI) is obtained by filtering through a linear phase symmetric impulse response while the other output (e.g., h2) is obtained by filtering through a linear phase anti-symmetric impulse response. In the present system, Hilbert filter 328 functions as a real input, complex output, digital filter intended for the QAM modulation to split the received signal into its real and imaginary components. For the VSB mode, the Hilbert filter will pass only the real component (hI) of the received signal since the modulation is one dimensional. For the VSB mode, the receiver is programmed to ignore the h2 imaginary component. This is achieved based on configuration data detailing a VSB system held in the host microprocessor 400. Although not detailed, it should be appreciated that, in response to a VSB control signal 401 applied to the host microprocessor 400 or to a QAM control signal 403 applied to microprocessor 400, the microprocessor 400 controls the proper operation of the function.

The LO2 adjustment circuit 325 also supplies a signal r1 to summer circuit 326. The signal rI represents the correction necessary to remove the residual frequency offset after LO2 has been adjusted to within 60 KHz of the nominal transmitter frequency. The signal on lead rI represents the supplemental angle to add to the fixed carrier angle to demodulate the output of the Hilbert filter completely to baseband. The fixed carrier

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angle is produced by fixed carrier demodulator table circuit 324 which produces an output signal r2 supplied to summer (adder) network 326. The adder network 326 functions to sum the rl and r2 signals and produces output signals sl and s2 which are the sine and cosine of the composite angles employed for demodulation; which demodulation is accomplished at the sampling rate.

The signal rl may be generated via phase locked loop (PLL) circuitry located within LO2 adjust circuit 325. Normally, this circuitry cannot handle as much offset as is anticipated in LO2 (approximately 1 MHz). Thus, prior to operating this loop, the majority of the offset is removed via signal Z. The signal r2 will be generated via a table look-up scheme, detailed below.

The two outputs, sl, s2, from summer 326 are applied to demodulator 323 whose other inputs are the hl and h2 outputs from Hilbert filter 328. For the VSB mode, only the h1 output is used; h2 is set to zero. Demodulator 323 produces at its output baseband signals I and Q which are coupled via lines 62 and 61, respectively, to timing recovery circuit 321 and AGC circuit 322.

The I and Q signals produced on lines 62 and 61, respectively, are the digital equivalent of the I and Q signals produced at the outputs of the ADC 29 and 30 in the prior art system of FIG. 1.

The I and Q signals produced in accordance with the preferred embodiment have the following advantages:

1 - I and Q have exactly 90 degrees phase difference at all frequencies for every implementation. This is in contrast to the prior art approach where there is approximately 90 degrees phase difference and there is no consistent phase difference between multiple receivers of the same design. This is due to the fact that, in the preferred embodiment, the I and Q signals are derived via a digital Hilbert filter, whereas in the prior art, I and Q are derived via analog circuit means; and

2 - I and Q have a precisely controlled amplitude characteristic as compared to FIG. 1 where component tolerances cause inconsistent amplitude variations between multiple implementations.

The timing recovery circuit 321 processes the received I and Q signals as inputs because the transmit signal for QAM was generated using the transmitted I and Q signals. After processing, the timing recovery circuit, 321, generates clock signals which are locked to the transmitter clock signals.

Timing recovery circuit 321 produces a 43.04 MHz sampling signal applied to S/H 51 via line 90 and a 21.52 MHz sampling signal applied to ADC 52 via line 80. The 43.04 MHz clock may be generated via a 43.04 MHz voltage controlled crystal oscillator with a control input generated internal to block 321. The 21.52 MHz clock signal may be generated by a simple divide by 2 circuit to which the 43.04 MHz clock is applied.

AGC 322 produces an output signal "U" which is coupled via line 75 to AGC control circuit 40. Signal U is a digital signal as compared to the analog control of the prior art. The digital signal, U, can be utilized by the AGC circuit 40 by a serial transfer of the bits representing the signal into, for instance, a multiplying D/A converter (MDAC) which is a standard component for digitally controlled AGC's.

In the system of Figure 2, the Timing Recovery circuit 321 and the AGC 322 circuit are preceded by a digital demodulator 323 to baseband system which includes a fixed carrier demodulator look-up table circuit 324 [$n(2\pi/8)$ for VSB and $n(2\pi/4)$ for QAM] and an LO2 adjustment circuit 325 for correcting any frequency offset of LO2. For the VSB system, the LO2 adjustment scheme is a digital pilot tone tracking loop. The QAM system will also be required to adjust LO2 but may not include a pilot tone for that purpose. The QAM scheme may be completely data directed.

The total angle which is the sum of the fixed carrier and any offset produced by the LO2 adjustment circuit is summed at summer 326. The design of the LO2 adjustment circuit for VSB could take a similar form to the analog loop shown in Fig. 1 through blocks 24, 25, 26 and 27 or could include variations. The QAM loop may be derived without the aid of a pilot tone.

Consider first, operation for the VSB system. Tracking the pilot tone (PT), indicated by a vertical pointing arrow in FIG. 3, is accomplished digitally using a digital phase tracking loop located within LO2 adjust circuit 325 in the demodulator chip 320. The LO2 adjust circuit 325 outputs a coarse adjustment control (Z) which is applied via line 70 to LO2. That is, the digital phase pilot tone tracking loop attempts to remove frequency offset on the pilot within a certain frequency range (e.g., 60 KHZ). If the offset proves to be greater than 60 KHz, the tracking loop can bring up LO2 via control line 70 in 60 KHz steps until the offset is within 60 KHz. The coarse and fine adjustments (fine adjustments are made by means of signals rl and r2 supplied to demodulator 323) can be saved on a channel change circuitry (a RAM) in a memory circuit located at the demodulator chip host microprocessor 400 for subsequent use. This feature was not possible with the prior art analog phase tracking loop.

Consider next that the preferred system is intended to demodulate digitally two different carriers. One carrier for a VSB system and the other carrier for a QAM system. It is desirable to select an Intermediate frequency (IF) which allows very simple digital demodulation for both schemes. Since, in this application, the QAM and VSB baud rates are related by a factor of 2 (5.38MHz and 10.76MHz, respectively), it is desirable to sample the A/D converter 52 at a 21.52 MHz sampling rate for either VSB or QAM. To satisfy the Nyquist criteria, prior to sampling there is inserted a 10.76 MHz anti-aliasing low pass filter (AALPF) 53. This means that the sample

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and hold circuit 51 must shift the spectrum from 37.66 MHz as shown in waveform S/H OUT of FIG. 3.

The centre frequency for the IF bandpass filter 16 was selected to be 37.66 MHz to enable the digital demodulation by the fixed carrier frequency to be done by very simple angles. The demodulation by the carrier possesses the form $e^{(-jwcnTs)}$; where wc is equal to $2\pi fc$, and fc is the carrier frequency; n is an integer; and Ts is equal to 1/fs; where fs is the sampling rate or frequency at which the ADC 52 is sampled.

Note that the demodulation angle used to perform the final conversion of the sampled data to the baseboard signal is a function of $e^{(-jwcnTs)}$ which is equal to: $\cos w_c nTs - j \sin w_c nTs$; where $w_c = 2\pi fc$ and $Ts = 1/fs$. By selecting fs to be equal to Kfc where K is a rational number, the expression for the demodulation angle reduces to $e^{(-j2\pi n/K)}$.

For VSB, fc is 2.69 MHz and for QAM, fc is 5.38 MHz. For both systems, fs is 21.52 MHz. Therefore, the value of K for QAM is equal to 4 and K for VSB is equal to 8, whereby the demodulation angle for QAM is a function of $n(2\pi/4)$ and the demodulation angle for VSB is a function of $n(2\pi/8)$. For this illustrative example, the values of the demodulation angle for QAM and VSB can be calculated for different values of n as set forth below:

For QAM:		
n	cos (2π/4) (n)	sin (2π/4) (n)
1	0	1
2	-1	0
3	0	-1
4	1	0

For VSB:		
n	cos (2π/8) (n)	sin (2π/8) (n)
1	cos 45= $\sqrt{2/2}$	$\sqrt{2/2}$
2	90 = 0	1
3	135 = $\sqrt{2/2}$	$\sqrt{2/2}$
4	180 = 1	0
5	225 = $\sqrt{2/2}$	- $\sqrt{2/2}$
6	270 = 0	1
7	315 = - $\sqrt{2/2}$	- $\sqrt{2/2}$
8	360 = 1	0

By the appropriate selection of the frequency relationship of fc to fs, demodulation angles are produced which are very easy to implement via table look up with very small table sizes. The QAM case can merge the eight values of sine and cosine, shown above, to only 5 distinct values by adding a "1" to the fifth row of the sine table and noticing that cosine can be generated from the sine table by adding 2 to the sine pointer within the table. Thus, QAM requires a table of only 5 values for both sine or cosine, whose values will be either 0 or ±1. Similarly, the VSB case requires a table of 10 values for sine or cosine which will be either 0, ±1 or ± 2/2. These tables may be stored in a ROM 300 located within fixed carrier demodulator table 324 which is accessed depending on the mode (VSB or QAM) selected by the host microprocessor 400. Note that if a different IF frequency is selected (other than 37.66 MHz), the size of the required tables may change significantly.

The S/H sampling frequency (fSA) was selected to be 43.04 MHz so that the A/D (fSB) sampling clock could be derived from the S/H clock by a simple divide by 2 (21.52 MHz). It is advantageous to use 21.52 MHz as a sample clock because the desired symbol rates of the system are 10.76MHz and 5.38MHz for VSB and QAM, respectively. Not only will the symbol clock rate be easy to generate this way by dividing the 43.04 MHz clock by 4 or 8, but the resulting decimation by 2 is simple as well. That is, any symbol rate processing required by other receiver functions must decimate the sampling data stream by 2 or 4 for VSB or QAM, respectively. With the sampling and symbol rates selected, this means simply discard every other sample for VSB and 3 of every 4 samples for QAM for those processes that desire symbol rate input. If a different sampling rate was selected which was a rational ratio of the symbol rate [i.e., (n/m)(21.52)], then a more complex interpolation/ decimation approach at the input to symbol rate processing is required. Selecting the sample/symbol ratio by the preferred embodiment obviates the need for complex interpolation/decimation approaches.

It should be appreciated that the preferred embodiment may be used with any IF frequency by changing the S/H sampling rate. For example, assume that it is desired to use a standard 44 MHz IF filter instead of the 37.66 MHz filter 16. Then, the S/H must be operated at a sampling rate of 49.38 MHz (i.e., 5.38 MHz above the centre frequency of IF filter 16. The result would give a similar spectrum at the S/H output as is shown in FIG. 3. The AALPF output can then be sampled at the 21.52 MHz rate. However, there is now a disadvantage in that the 21.52 and 49.38 are not related by a simple ratio of two whole numbers such as 2:1 set for 43.04 and 21.52. The use of such a ratio would increase the complexity of the clock generating circuitry. Furthermore, a ratio such as this would increase the sampling clock jitter.

Consequently in systems embodying the invention it is preferred (although not necessary) to set the centre frequency of IF filter 16 at 37.66 MHz. Such a filter is not standard. But, present day technology permits such a filter to be designed in a surface acoustical wave (SAW) filter.

Further, if for instance analog NTSC TV were to coexist with the digital HDTV within the same TV set, it

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may not be desirable to sample the S/H at 43.04 MHz because of anticipated interference with the 44 MHz IF frequency currently used in the analog NTSC TV signal. If it is undesirable to change the analog NTSC IF frequency to coincide with the digital IF frequency of 37.66 MHz, a 75.334 MHz voltage controlled crystal oscillator could be incorporated which, when divided by 2, creates a S/H sampling rate of 37.66 MHz. This frequency (75.334 MHz) will no longer coincide with the analog NTSC IF frequency range. Also, instead of using a 37.66 MHz IF frequency for the digital HDTV, it must be changed to 32.39 MHz to obtain the resulting AALPF spectrum in Fig. 3. Now, to generate the 21.52 MHz sampling clock requires a rational rate multiplier of 2/7 times the master crystal oscillator frequency (i.e., 75.334 MHz). This is more complex than a simple divide by 2 used for the 43.04 MHz sample and hold rate and may create higher clock jitter on the sample clock.

In the system of Fig. 2, the AGC control 40 is derived from a combination of analog IF circuitry and the digital AGC block 322 which follows the A/D converter 52. The IF circuitry supplements the AGC because of the problems that may arise if the A/D converter 52 were to saturate in the absence of the IF AGC control. The delay to reacquire AGC will be shorter using this approach as compared to a completely digital AGC approach.

As shown in Fig. 4, other embodiments may use an alternative approach to circuit 50. The alternative is to use a 43.04 MHz A/D converter with its own internal sample and hold circuitry and digital conversion operating at 43.04 MHz. For example, converter circuit 501 in Fig. 4 would replace converter circuit 50 in Fig. 2. In Fig. 4, an N-bit ADC 521 is connected at its input (H) to the output of amplifier 18 to receive the IF signal, elM, and its N-bit output (P) is supplied to the input of a Hilbert filter 328. Note that this configuration does not require an AALPF or external S/H as did FIG. 2. It also does not require the AALPF 28, 31 in the configuration of Fig. 1. This is because FIG. 4 has only one sampling process, not two, as in FIG. 2. However, ADC 521 of Fig. 4 is capable of operating at twice the frequency of ADC 52 in Fig. 2. The timing recovery circuit 321 supplies a 43.04 MHz clocking sampling signal to ADC 521.

The elM IF signal sampled by ADC 521 is the 6 MHz bandwidth IF OUT signal shown in Fig. 3 having a centre frequency (fc) of 37.66 MHz extending +3 MHz up to 40.66 MHz and ranging down by 3 MHz to 34.66 MHz.

By sampling the IF signal at a rate of 43.04 MHz, a band of signals is produced extending between -8.07 MHz and -2.69 MHz with a centre frequency of -5.38 MHz. Applicant recognized that the "negative" IF frequency component generates a mirror image lying between 2.69 MHz and 8.07 MHz with a centre frequency of 5.38 MHz. Furthermore, other repetitions are formed by the 43.04 MHz sampling, as shown by waveform S/H OUT in FIG. 3. Recall that in FIG. 2, since a first sampling takes place at 43.04 MHz and a second sampling takes place at a rate of 21.52 MHz, all analog energy must be removed beyond 10.76 MHz by means of AALPF 53. By contrast, in the Fig. 4 system, the only sampling done is at 43.04 MHz and since aliasing is not evident at the S/H OUT, no AALPF is required. Thus, for the configuration of Fig. 4, since there is only one sampling process, the spectrum labelled S/H OUT is actually the spectrum of the output of the A/D converter. Further, since there is no overlap around 1/2 the sampling frequency [1/2(43.04)=21.52MHz), no aliasing is evident.

Applicant also recognized that ADC 521 need not be sampled at a rate of twice the highest frequency of 40.66 MHz to satisfy the Nyquist criteria and to produce a desired baseband signal of the type shown in waveform S/H OUT in Fig. 3.

It is important to note that in the preferred systems and circuits, it is the IF signal which is sampled. Thus, only first and second local oscillators and only two mixers are needed to down convert the IF input signal to the intermediate frequency band which IF band is then sampled to demodulate the I, Q signals of interest. The I and Q signals are produced by the same circuitry whereby the phase and amplitude of the I and Q signals are not affected by the values of different components along different paths.

The disclosures in United States patent application no. 08/544,244, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

Claims

1. A radio frequency (rf) receiver comprising:

 an input terminal (9) operable to receive one or more of a number of different digitally modulated rf input signals;
 converting means (10-18) including an input and an output;
 means coupling the input of said converting means to said input terminal for down converting the rf input signal and for producing at the output of said converting means an intermediate frequency (IF) signal; and
 sampling means ('50) including an input coupled to the output of said converting means for digitally sampling the intermediate frequency signal and including an output for producing thereat base band signals in response to the rf input signals.

2. A radio frequency (rf) receiver as claimed in claim 1,

 wherein said input terminal (9) is operable to receive one or more of a number of different digitally modulated rf input signals including quadrature amplitude modulated (QAM) and vestigial side band (VSB) rf input signals; and

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wherein said sampling means includes means for producing at its output an in-phase (I) base band signal and a quadrature (Q) base band signal in response to a QAM rf input signal and for producing an in-phase (I) baseband signal in response to a VSB rf input signal.

3. A radio frequency (rf) receiver as claimed in claim 1 or 2, wherein said converting means includes:

a first mixer (MX1) and a second mixer (MX2), each mixer including an input and an output;
a first local oscillator (LO1) and a second local oscillator (LO2), each local oscillator including an output at which is producible a frequency signal;
means coupling an output of the first local oscillator and the rf input signals to the input of the first mixer;
means coupling the output of the first mixer to an input of a first bandpass filter (BPF1) having a first centre frequency (fcl) and a bandwidth of Bhz to produce at an output thereof a first output signal (fol) having a first centre frequency of fcl with a bandwidth of Bhz;
means coupling the output of the first bandpass filter and an output of the second local oscillator to an input of the second mixer for down converting the rf signal; and
means coupling the output of the second mixer to an input of a second bandpass filter having a second centre frequency (fc2) and a bandwidth of Bhz, the second bandpass filter including an output, providing the output of the first converting means, for producing thereat an intermediate frequency signal whose centre frequency is substantially equal to fc2 and whose bandwidth is substantially equal to Bhz.

4. A radio frequency (rf) receiver as claimed in claim 1, 2 or 3, wherein the sampling means includes:

a sample and hold circuit (51) including an input, an output and a clocking input;
a low pass filter (53) including an input and an output; and
an analog-to-digital converter (52) including an input, an output and a clocking input;
means coupling the input of the sample and hold circuit to the output of the converting means and the output of the sample and hold circuit to the input of the low pass filter;
means coupling the output of the low pass filter to the input of the analog-to-digital converter; and
means for applying a sampling signal having a frequency f3 to the clocking input of the sample and hold circuit and for applying a sampling signal having a frequency f4 to the clocking input of the analog-to-digital converter; and wherein f3 is a rational multiple of f4.

5. A radio frequency receiver as claimed in claim 1, 2 or 3, wherein said sampling means (501) includes solely a single analog-to-digital converter (521) including an input coupled to the output of said first converting means for digitally sampling said IF signal and producing baseband signals.

6. A radio frequency receiver as claimed in claim 1, 2 or 3, wherein the sampling means includes an analog-to-digital converter (52) including a signal input port, a signal output port and a clocking input for the application thereto of a sampling signal; and

wherein the signal input port of the analog-to-digital converter is coupled to the output of the converting means and the signal output port of the analog-to-digital converter is coupled to a demodulator circuit (320).

7. A radio frequency receiver as claimed in claim 6, wherein the sampling means includes means for applying a sampling signal to the clocking input of the analog-to-digital converter, the sampling signal having a rate which is substantially equal to, or greater than, the sum of the centre frequency (fc2) of the second bandpass filter plus either one half the bandwidth of the QAM signal or one half the bandwidth of the VSB signal.

8. A radio frequency receiver as claimed in any one of claims 4 to 7, wherein the centre frequency of the first bandpass filter minus the frequency of the signal at the output of the second local oscillator coupled to the second mixer is equal to the centre frequency of the second bandpass filter.

9. A radio frequency receiver as claimed in claim 8, wherein the frequency of the sampling signal applied to the sample and hold circuit is equal to, or greater than, the sum of the centre frequency fc2 of the second band pass filter plus a frequency fA; where fA is equal to either one half of the bandwidth of the QAM signal or one half of the bandwidth of the VSB signal.

10. A radio frequency receiver as claimed in claim 1, 2 or 3, wherein said sampling means includes an analog-to-digital converter (ADC) having a signal input coupled to the output of BPF2, a signal output and a clocking input, and wherein a sampling signal is applied to the clocking input for sampling the signal at the input at a rate (fs) which is greater than the centre frequency (fc2) of the BPF2 plus B/2 Hz.

11. A radio frequency receiver as claimed in any one of

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claims 4 to 10, wherein the output of the analog-to-digital converter is supplied to the input of an Hilbert filter (328) for producing at the output of the Hilbert filter real and imaginary components of the sampled signals.

12. A radio frequency receiver as claimed in claim 11, wherein the output of the Hilbert filter is applied to a or the demodulator for producing I and Q baseband signals responsive to a QAM rf input signal and an I baseband signal responsive to a VSB rf input signal.

13. A radio frequency receiver as claimed in claim 12, wherein the demodulator (320) includes means for digitally demodulating the carrier signals and completing the transfer of the received signal to baseband at the output of the demodulator.

14. A radio frequency receiver as claimed in claim 11, 12 or 13, including means for adjusting the frequency of the second local oscillator; said adjusting means including a local oscillator adjust circuit (325) comprising an input coupled to the output of the Hilbert filter and an output coupled to the second local oscillator for adjusting its frequency.

15. A radio frequency (rf) receiver comprising:

an input terminal (9) operable to receive one or more of a number of differently modulated rf input signals including quadrature amplitude modulated (QAM) and vestigial side band (VSB) rf input signals;
first converting means (10-18) including an input coupled to said input terminal and operable to down convert said rf input signals and including an output for producing thereat an intermediate frequency signal; and
second converting means (50, 320) including an input coupled to the output of the first converting means and sampling means and demodulating means for digitally sampling the intermediate frequency signal and for producing a baseband signal corresponding to the particular rf input signal received.

16. A radio frequency (rf) receiver as claimed in claim 15, wherein said second converter means is responsive to said intermediate frequency signal for producing at its output an in-phase (I) base band signal and a quadrature (Q) base band signal in response to a QAM rf signal and for producing an in-phase (I) baseband signal in response to a VSB rf signal.

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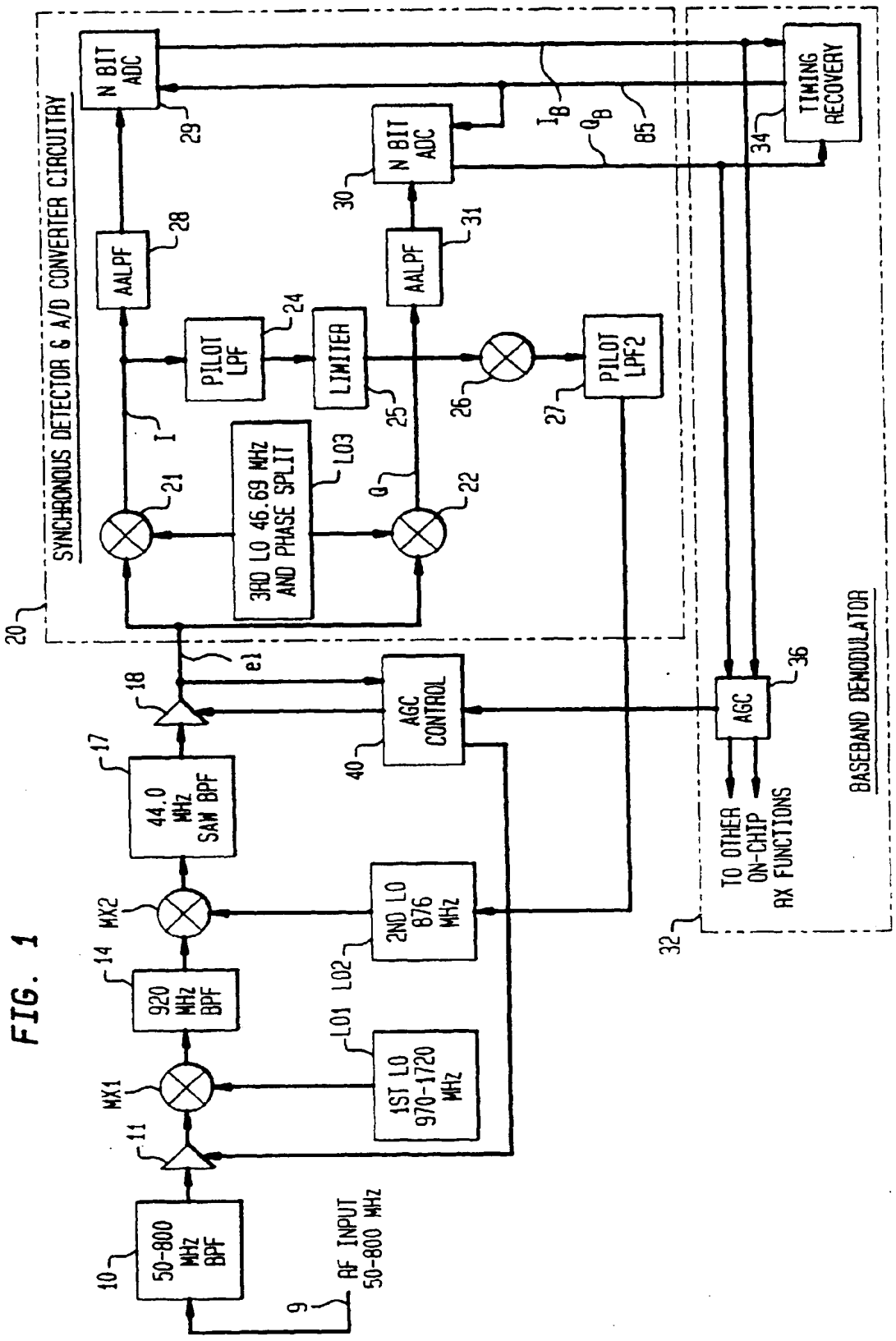


FIG. 1

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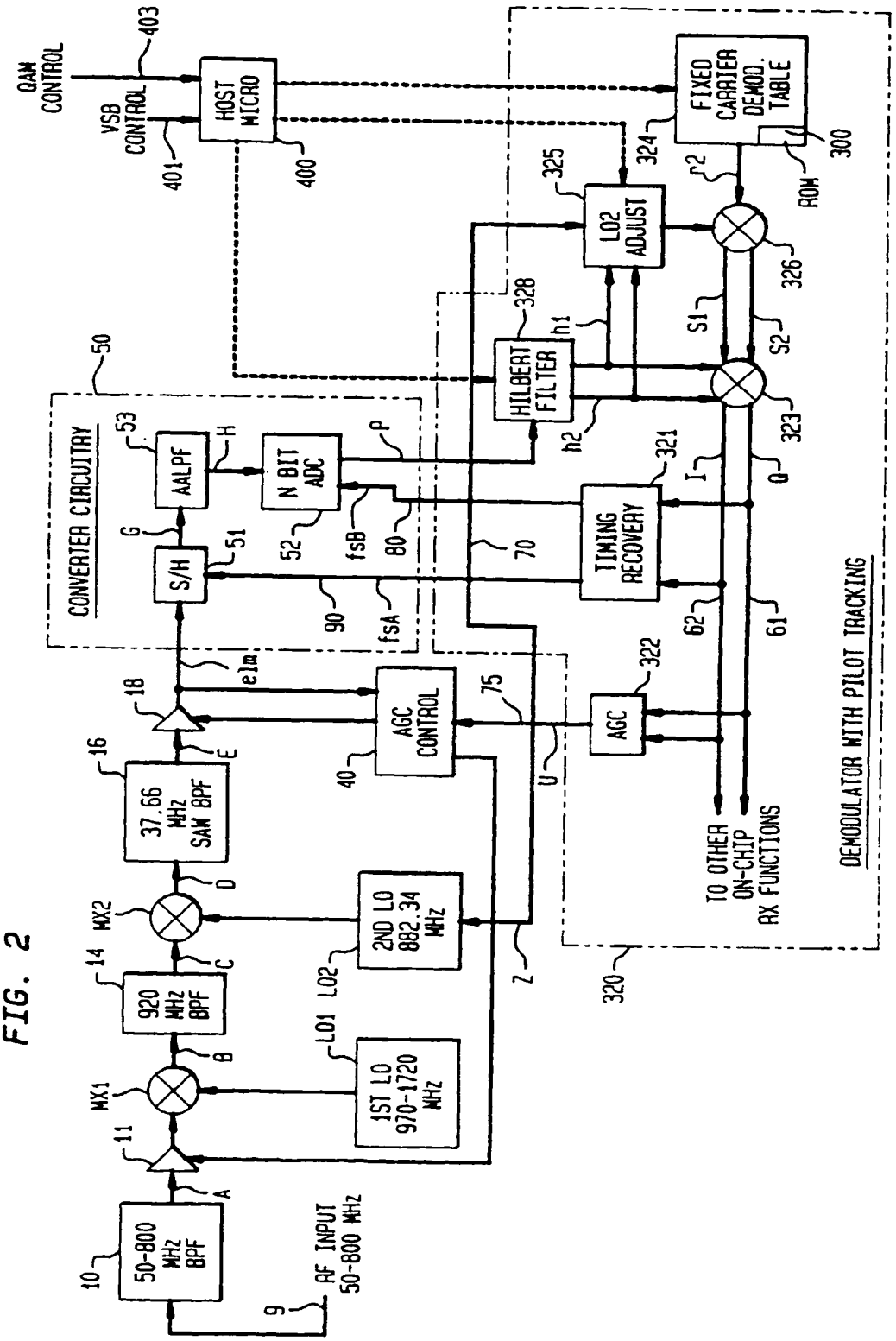


FIG. 2

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FIG. 3A

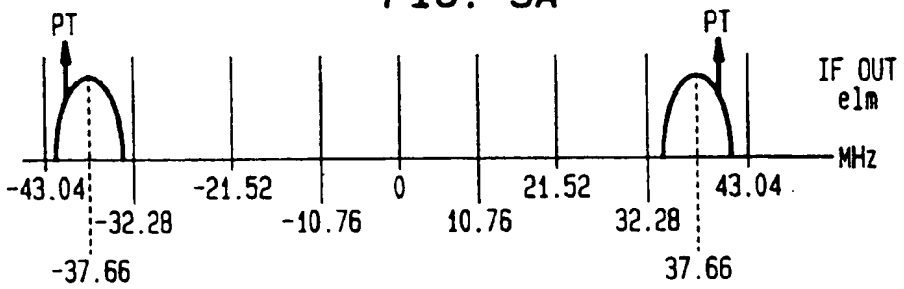


FIG. 3B

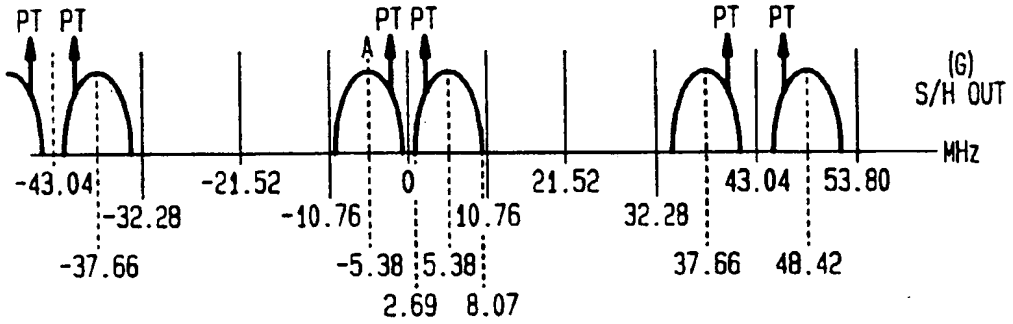


FIG. 3C

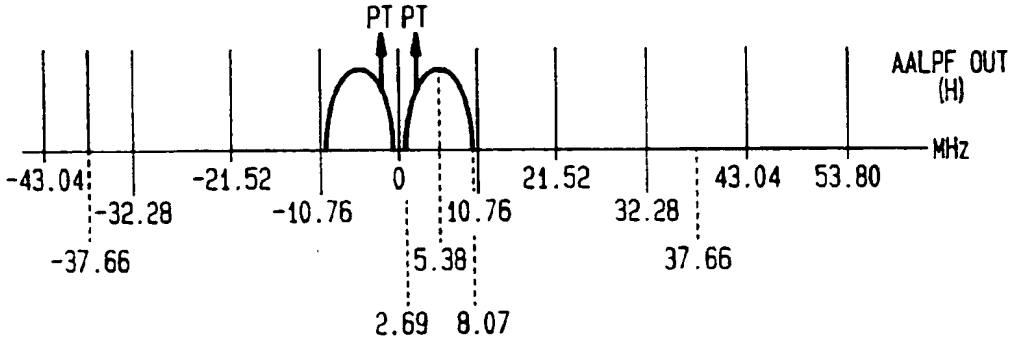
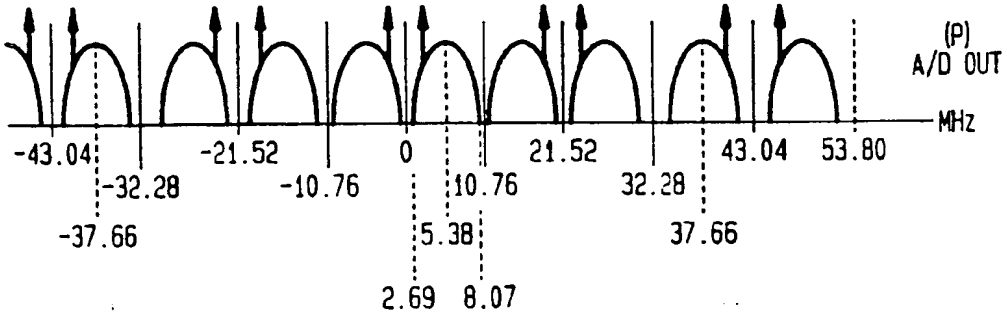
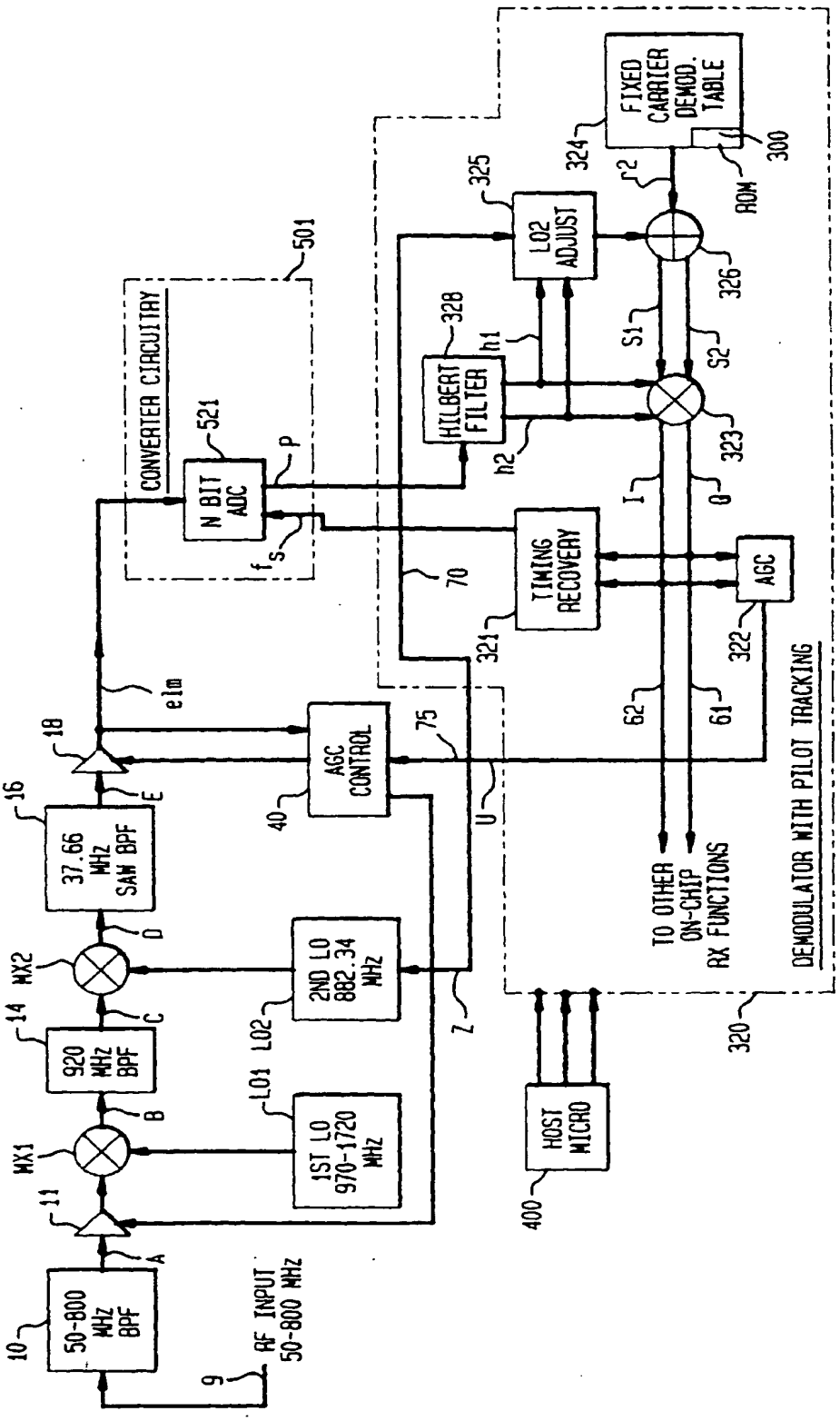


FIG. 3D



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FIG. 4



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Application Number
EP 96 30 7468

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	ELECTRONIC DESIGN, vol. 39, no. 10, 23 May 1991, pages 67-68, 70, 73-75, 78, XP000234611 GROSHONG R. ET AL.: "Undersampling techniques simplify digital radio" * page 68, middle column, line 13 - line 33 *	1,3, 5-10,15	H04N5/46 H04L27/06 H04L27/38
Y	* page 73, left-hand column, line 16 - line 30 *	2,4,16	
A	* figures 2,3 *	13	
X	NTC 78. CONFERENCE RECORD OF THE IEEE 1978 NATIONAL TELECOMMUNICATIONS CONFERENCE, BIRMINGHAM, AL, USA, 3-6 DEC. 1978, vol. 1, NEW YORK, NY, USA, IEEE, USA, pages 2.1/1-5, XP002022928 GRANT T. L.: "A versatile microprocessor-controlled hybrid receiver" * abstract * * page 2.1.1, right-hand column, line 17 - line 30 *	1,3,6,15	
Y	* page 2.1.2, left-hand column, line 2 - line 7 * * figures 1,2 *	2,4,16	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04L H04N
X	EP-A-0 667 712 (HITACHI) 16 August 1995 * column 1, line 3 - line 22 *	1,3,5,6, 15	
Y	* column 6, line 9 - line 20 * * column 13, line 7 - line 48 *	2,16	
A	* figure 8 *	13,14	
X,P	US-A-5 506 636 (PATEL ET AL.) 9 April 1996	1,3-6, 11,13,15	
Y	* abstract; figures 1-3 *	2,12,16	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 January 1997	Ghigliotti, L

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	EP-A-0 574 273 (TOKYO SHIBAURA ELECTRIC CO.; TOSHIBA AVE KK (JP)) 15 December 1993 * column 15, line 28 - line 57 * * column 18, line 8 - line 28 * * figure 11 *	2,12,16	
Y	EP-A-0 458 452 (TECHNOPHONE) 27 November 1991 * page 2, line 22 - line 24 * * page 3, line 13 - line 41 *	4	
A	* figure 2 *	7-11	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 January 1997	Ghigliotti, L

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